13.7 A 1.5V 200MS/s 13b 25mW DAC with Randomized Nested Background Calibration in 0.13µm CMOS

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On-chip calibration techniques enable the realization of compact current-steering DAC-modules with 12b+ resolution [1-4]. While foreground calibration [1, 2] is only performed once, e.g., at start-up, calibration in background periodically re-trims the unit current sources of the converter [3, 4]. Therefore, it not only removes static mismatch errors of the DAC elements, but also tracks time-varying errors, mainly related to slowly changing bias conditions and on-die temperature fluctuations. In this work, 2 background calibration techniques are introduced to comply with low supply voltage and low-power operation: Nested calibration trims all DAC segments independently while randomization of the refresh period attenuates the spurious tones generated by the periodic calibration process.

Figure 13.7.1 shows the architecture of the proposed 13b DAC. It is segmented into a 6b unary MSB array, a 2b unary upper-LSB (ULSB) array, and a 5b binary lower-LSB (LLSB) array. The MSB sources are directly trimmed by sequentially comparing their value with a constant reference current, I_{REF}, and forcing the current difference to zero. Accurate current-splitters for the generation of lower segment currents from a trimmed MSB source [1, 3] are avoided, because they limit the maximum output voltage swing by stacking at least one additional transistor between the current source and the current switch. Instead, nested background calibration trims the segment boundaries of independent ULSB- and LLSB-arrays by matching the sum of the currents in any of the lower segments to the smallest element in the next higher previously trimmed segment. The current-source matching within the lower segments is guaranteed by proper sizing. To achieve uninterrupted foreground operation, appropriate redundancy is introduced.

After sequentially calibrating the 63+1 MSB unit cells, the sum of 4 ULSB-A unit cells is compared with the reference current I_{REF} and the total current in the ULSB-A array is matched to the MSB unit current. Meanwhile, the ULSB data is processed by a redundant ULSB-array (ULSB-B). Next, the sum of 3 previously calibrated ULSB-A cells and the total current in the LLSB-A array (plus one dummy LSB-current) is compared with the reference current I_{REF} and the total current of the LLSB-A array is matched to the ULSB unit current. Meanwhile the second LLSB-array (LLSB-B) processes the LSB-data. ULSB-A/B and LLSB-A/B are calibrated in turn.

Figure 13.7.2 shows the analog calibration loop in more detail. The current to be calibrated, e.g., an MSB current or the sum of 4 ULSB currents, is switched to node A and compared with I_{REF}. By controlling the gate-source voltage of the variable current-source transistor MV, the difference between the input current at node A and I_{REF} is forced to zero. The capacitor CS stores the value of the trimmed gate-source voltage of MV until the next calibration cycle [3]. The LLSB arrays, instead, are calibrated indirectly by controlling the bleeding current in transistor MB, located in the LLSB biasing (LLSB-CALBIAS).

Due to its periodic nature, background calibration can easily generate spurious tones in the output signal at multiples of the refresh-cycle frequency. One solution is to implement floating current cells and apply backside calibration with the current cell concurrently working in normal operation [4]. Because in this case the periodic switching-in and out of DAC elements into calibration mode and back is not necessary, adequate attenuation of the calibration tones can be achieved. However, due to voltage-headroom reasons, these architectures require a current-folding output stage that at least triples the static power consumption of the DAC.

In this design the spurious tones generated by the periodic calibration process are spectrally shaped by introducing time-domain randomization of the trimming interval. In this way, discrete calibration spurs are converted into wideband noise. The length of the trimming interval for the single-unit current source, the calibration period T_{CAL}, consists of a fixed time interval T_{FIX} and a random time interval T_{VAR}. As shown in Fig. 13.7.2, T_{CAL} is generated with a programmable counter that is preloaded with the sum of a fixed number N_{FIX} and a random number N_{VAR}=[0; $N_{VAR,MAX}$], coming from a maximum-length LFSR and updated before every calibration period. T_{CAL} is therefore a random time interval in the range [T_{FIX}; T_{FIX}+$T_{VAR,MAX}$]. The lower boundary T_{FIX} is dictated by the settling time of the analog calibration loop, while the upper boundary T_{FIX}+$T_{VAR,MAX}$ is limited by the leakage of the charge stored on capacitor CS.

Figure 13.7.3 shows the measured effect of the calibration-period randomization on the magnitude of the tone at the refresh-cycle frequency for different degrees of randomness. Without randomization, the biggest calibration spur is found at -80.8dBFS (dB referred to full-scale) and would limit the SFDR of the calibrated converter. When the randomization of the calibration period is activated and $T_{VAR,MAX}/T_{FIX}$ is gradually increased, then the calibration tone decreases. An optimum is found when the 2 time-bases are about equal ($T_{VAR,MAX}$=T_{FIX}), at which setting the fundamental calibration spur is attenuated by more than 20dB, down to -102.6dBFS. If $T_{VAR,MAX}$ is chosen too small, then the spectral shaping of the calibration tones is not effective while a very large $T_{VAR,MAX}$ makes the overall refresh cycle too long.

Figure 13.7.4 shows the measured linearity improvement when using different degrees of nested calibration. Without calibration, the THD for a 1MHz sine wave sampled at 200MHz is limited by the static mismatch of the current sources to typically -66dBc. Calibrating only the MSB array, the THD improves to -76dBc. Finally, when calibrating all 3 DAC segments, the THD reaches -80.7dBc. Figure 13.7.5 shows the measured SFDR for a clock rate of 100 and 200MS/s. The low-frequency SFDR with background calibration turned on is 83.7dB for both update rates. Close to the Nyquist frequency, the SFDR reduces to 67.5 and 54.5dB for a clock rate of 100 and 200MHz, respectively.

Figure 13.7.6 shows the die micrograph. The prototype converter is fabricated in a standard 1P6M 0.13µm CMOS technology. When clocked at 200MHz, the total power consumption of the DAC is 25mW from a 1.5V supply. The key performance data are summarized in Fig. 13.7.7.

References:

[1] W. Schofield, D. Mercer, and L. S. Onge, "A 16b 400MS/s DAC with <-80dBc IMD to 300MHz and <-160dBm/Hz Noise Power Spectral Density," *ISSCC Dig. Tech. Papers,* pp. 126-127, Feb., 2003.
[2] Y. Cong and R. L. Geiger, "A 1.5-V 14-bit 100-MS/s Self-Calibrated DAC," *IEEE J. Solid-State Circuits,* vol. 38, pp. 2051-2060, Dec., 2003.
[3] D. W. J. Groeneveld, H.J. Schowenaars, H.A.H. Termeer, et al., "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," *IEEE J. Solid-State Circuits,* vol. 24, pp. 1517-1522, Dec., 1989.
[4] Q. Huang, P.A. Francese, C. Martelli, et al., "A 200MS/s 14b 97mW DAC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 364-365, Feb., 2004.

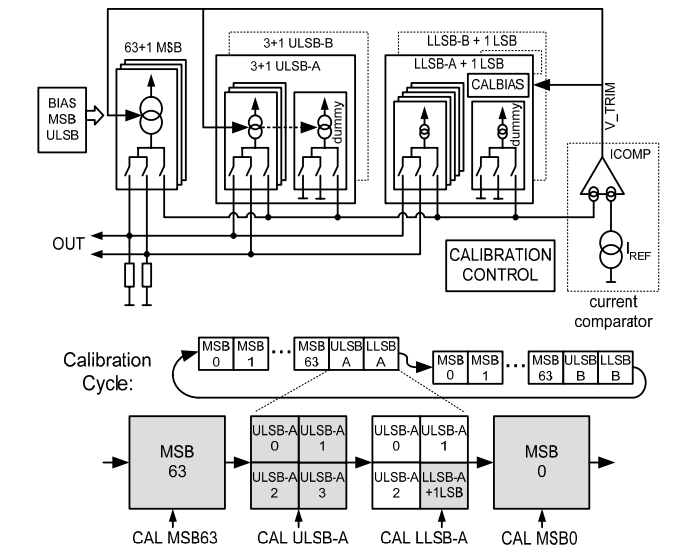

Figure 13.7.1: DAC with nested background calibration.

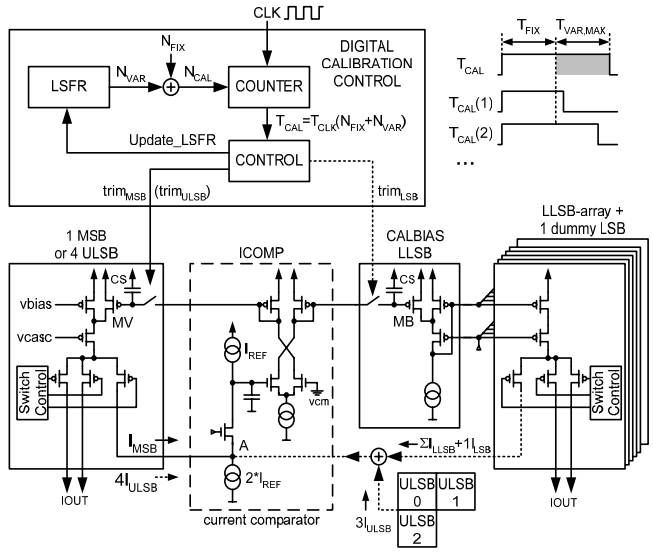

Figure 13.7.2: Randomized analog calibration.

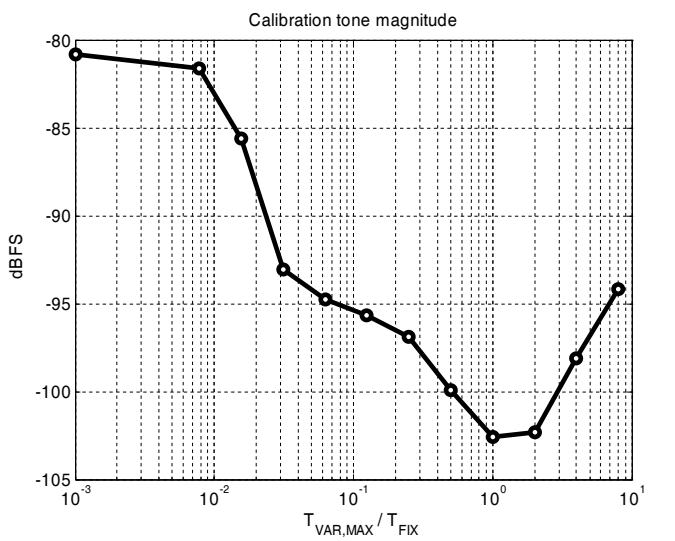

Figure 13.7.3: Attenuation of calibration spurs.

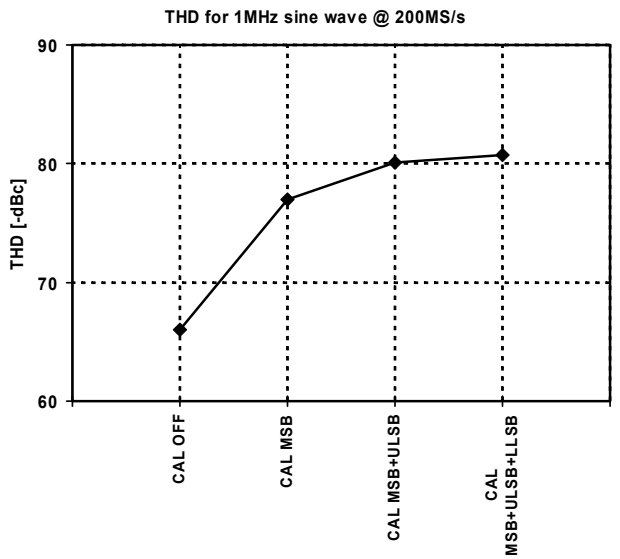

Figure 13.7.4: THD with nested background calibration.

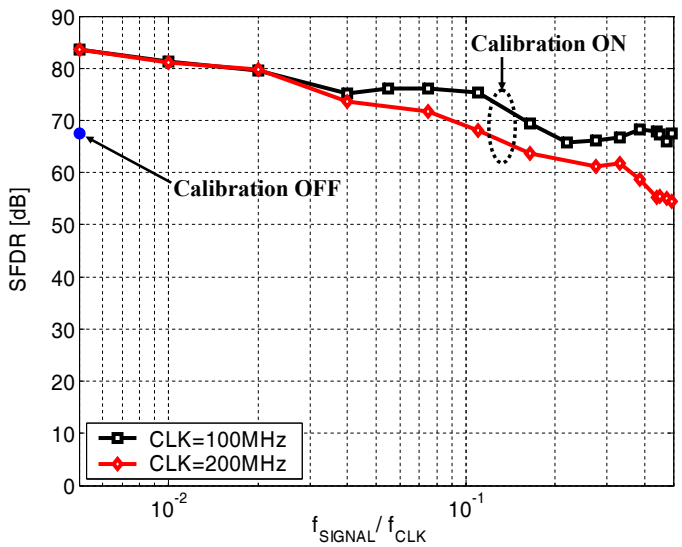

Figure 13.7.5: SFDR versus signal frequency.

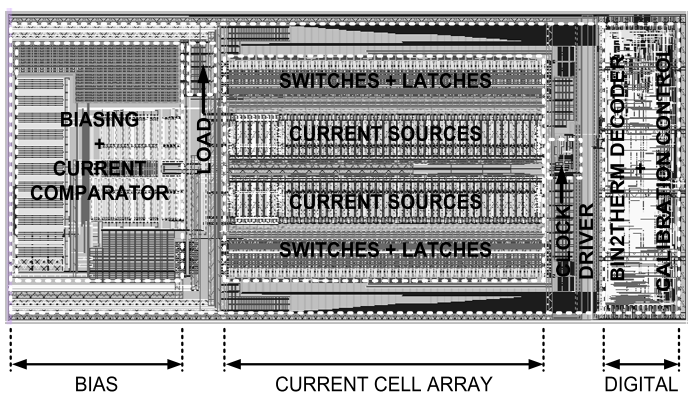

Figure 13.7.6: Die micrograph.

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Process	0.13µm CMOS 1P6M
Supply	1.5V (analog + digital)
Max. clock rate	200MHz
Power consumption (analog + digital)	25mW @ 200MS/s 19mW @ 100MS/s
SFDR @ f_{SIG} = 1MHz	83.7dB
SFDR @ $f_{SIG} \sim f_{CLK}/2$	67.5dB @ 100MS/s 54.5dB @ 200MS/s
Full-scale output current	5mA
Max. output swing	$1V_{pp\text{-}diff}$

Figure 13.7.7: Key performance data.

